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ECe 3200-01 Lab 12

The Differential Amplifier Stage

**Objective:**

The purpose of this lab is to construct a DC coupled differential amplifier, by using a pair of matched NPN-BJTs. Then the performance characteristics will be measured with two types of current biasing schemes. Next the differential (AD) and common mode (ACOM) voltage gains and other parameters will be measured with each scheme. The results of the measurements will be compared versus the equations derived from the circuit theory. As a result, we will learn how to design the circuit to meet the specifications.

**Introduction:**

A differential amplifier is a directly coupled active circuit which has two independent input drives (V1 & V2) and usually a single dependent output (Vo). One input (V1) is called the non-inverting input and the other (V2) as the inverting one. The output is generally the product of the non-inverting (A1) and inverting (A2) gains of each input. As a result assuming linearity the total output, Vo, by superposition will be equal to:

Vo = A1 V1 – A2V2 ………… 1

However, under a large signal condition, Vo, will be a nonlinear function of V1 and V2 in which case the equation 1 may not remain linear.

In a perfectly balanced differential amplifier A1 = A 2 ( = AD ) and hence the output will be equal to:

Vo = AD (V1 – V2) …………. 2

That is, the output will depend upon the ‘difference’ of the two input voltages and not the value of each individual voltage. Here AD is referred to as the differential gain and the output will be zero under the condition of V1 = V2 regardless of the value of V1 or V2.

However, due to lack of symmetry in the characteristics of the building components

generally A1 ≠ A2 and hence there will be an output equal to:

Vo = (A1 – A2) VCOM ……….. 3

where V1 = V2 = Vcom, is called the common mode input.

Indeed, ACOM = A1 –A2, is called the common-mode voltage gain and it is the ratio of Vo /Vcom. In applications it is desirable to have a small ACOM ( ideally zero) in comparison to the AD.

The CMRR (common-mode rejection ratio) is defined as the ratio of AD to ACOM, which in terms of dB is:

CMRR = 20 log ( AD /ACOM ) …… 4

Typical CMRR in an operational amplifier can be between 80 to 120 dB , from its low to high performance end.

**Prelab:**

1. Reference to the circuit of fig.1 determine Rc and Re so that quiescent currents, IC1 = IC2 = 0.83 mA and Vo = 7.29 V when both inputs (V1 = V2 = 0 V) are grounded. Assume β = 100 for both transistors.
2. Using small signal hybrid-π model show that the small-signal differential voltage gain, AD , from input V1 to the output Vo is equal to:

AD ≈ gmRc / 2 ≈ 54.78 (5)

Where gm = Ic 1 or 2 / VT is the small signal transconductance of the transistors and

VT = 25 mV is the semiconductor thermal voltage.

1. Also show that the common-mode voltage gain, ACOM, is equal to:

ACOM ≈ Rc / 2 Re ≈ 0.295 ≈ 0.3 (6)

1. Show that the differential input impedance, Rin (Diff.), is equal to:

Rin (Diff.) ≈ 2 rπ ≈ 11 kΩ (7)

Where rπ = β / gm.

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**Procedure:**

Part 1 – Build the circuit of fig.1 with the values you have calculated in prelab 1. With V1&2 grounded measure Vo, Ic1, Ic2 and IRe. The currents can be determined by measuring the resistor voltage and then dividing by the corresponding resistor values.

VRe = 9.31 v, VRc1 = 2.785 v, VRc2 = 2.740 v, IC1 = 0.84 mA , IC2 = 0.83 mA ,

IRe = VRe / Re = 1.66 mA , Vo = 7.26 v (Theoretical Values)

Ic1 = 0.83 mA, Ic2 = 0.83 mA, IRe = 1.67 mA, Vo = 7.261V (Measured Values)

Diagram, schematic

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Explain if there is a difference between Ic1 and Ic2 .

Part 2 – With V2 = 0 (i.e. grounded) build the signal attenuator circuit with a 1 kΩ and a 10 Ω resistor to introduce the ac input v1(pp)= 25 mVpp at 5 kHz, to the circuit. The connection may change the DC voltage at Vo. If this happened adjust the signal generator DC offset voltage to compensate till Vo is restored to the value you measured earlier in part 1. Measure the AC output vo (pp) and its phase angle with respect to the input v1 .

v1(pp) = 25 mVpp , vo = 1.205 vpp ( @ collector of Q2) (Theoretical Value)

v1(pp) = 23.8 mVpp , vo = 1.14 vpp ( @ collector of Q2) (Measured Value)

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Calculate the differential gain, AD = vo(pp) / v1 (pp) = 1.205 Vpp/25 mVpp = 48.2, phase = 0o. (Theoretical value)

AD = vo(pp) / v1 (pp) = 1.205 Vpp/25 mVpp = 47.9 = 0o . (Measured value)

Part 3 – Now measure the second AC output at the collector of the opposite transistor (Q1) and its phase and determine the gain.

vo (pp @ Q1) = 1.204 Vpp , v1 (pp) = 25 mVpp

AD = 48.16, phase = 180 0

What is the major difference?

The major difference is that the differential gain at the collector of the opposite transistor (Q1) had a phase of 180, while the phase for the collector of transistor (Q2). Thus, the peak-peak output voltage at transistor (Q1) is negative, causing the gain to have a phase of 1800.

Part 4 – Now connect both inputs together and introduce a common signal to both inputs as v1,2 (pp) . Measure the output vo(com). The common mode voltage gain is:

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V1,2 (pp) = 25 mVpp common input, vo (pp) = vo (com) = 7.5 mVpp @ Q2 (Theoretical Value)

V1,2 (pp) = 23.824 mVpp common input, vo (pp) = vo (com) = 6.935 mVpp @ Q2 (Measured Value)

ACOM = vo(com) / v1, 2 (pp) = 0.3 (Theoretical Value)

ACOM = vo(com) / v1, 2 (pp) = 0.29 (Measured Value)

Since this gain is much smaller than AD you may need to increase v1,2(pp) amplitude to obtain a measurable output. Also, you may need to adjust the offset too to maintain the same DC levels.

Part 5- CMRR now can be calculated as:

CMRR (dB) = 20 log AD / ACOM = 20 log ( 48.2 / 0.3 ) = 44 dB (Theoretical Value)

CMRR (dB) = 20 log AD / ACOM = 20 log ( 47.9 / 0.3 ) = 44.35 dB (Measured Value)

Part 6 – Now restore the circuit to the same connection as you had it in part 2 of the experiment. Introduce the resistor Rg = 2.2 kΩ between the attenuator and the base of the transistor Q1. Make sure Vo (DC) remains the same as in part 1 by readjusting generators DC offset voltage. Measure the AC input current iin = (vg – v1)/ Rg the input impedance

Rin(Diff) will be fond from:

Rg = 2.2 k, vg = 30 mVpp , v1 = 25 mVpp , iin = (30 – 25 ) mVpp / 2.2 kΩ

= 0.005 mApp (Theoretical Values)

Rin (Diff) = v1 / iin = 25 mVpp / 0.005 mApp = 5 kΩ

Rg = 2.2 k, vg = 23.824 mVpp , v1 = 18.905 mVpp , iin = (23.824 – 18.905) mVpp / 2.2 kΩ = 0.005 mApp (Measured Values)

Rin (Diff) = v1 / iin = 23.824 mVpp / 0.005 mApp = 4.77 kΩ

Diagram, schematic

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Part 7 – IMPROVING THE CMRR

Now the current biasing resistor, Re, is replaced with a constant current source utilizing the transistor Q3. Three silicon diodes will bias the base of the transistor Q3 and Rx will establish the emitter and hence the collector current. This current source will supply the current necessary for the differential pair and in the meantime it will provide a much higher dynamic resistance than the original scheme with a single Re.

The value of Rx is designed so that the collector of Q3 will provide nearly the same current as before. Construct the circuit as shown in fig.2.

Measure AD and ACOM by using the same procedure as you used in part 1 through 5. It is not necessary to measure Rin. Make sure the circuit is biased correctly and for that the DC value of Vo should be close to the result in part 1.

Part 7-1

Diagram, schematic

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Part 7-2

vo(q4) = 1.1049 V, phase = 0o

Part 7-3

vo(q5) = -1.102 V, phase = 180o

Part 7-4

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Part 7-5

Theoretical Values:

Ic Q3 = 1.89 mA, Vo = 6.9 V – it is close to 7.26 V.

V1 (pp) = 25 mVpp , vo (pp) = 1.300 Vpp , AD = 1.3 Vpp / 25 mVpp = 52 .

Common mode result: v1,2(com) = 25 mVpp, vo­(com) = < 1mVpp may be 0.2 mVpp See photo)

AD = 1.3 Vpp/25 mVpp = 52 , ACOM = 0.2 mVpp / 25 mVpp = 0.008 (with current source)

CMRR = 20 log AD / ACOM = 20 log ( 52 / 0.008 ) = 76 dB

Measured Values:

Ic Q3 = 1.66 mA, Vo = 7.29 V – close to 7.26 V.

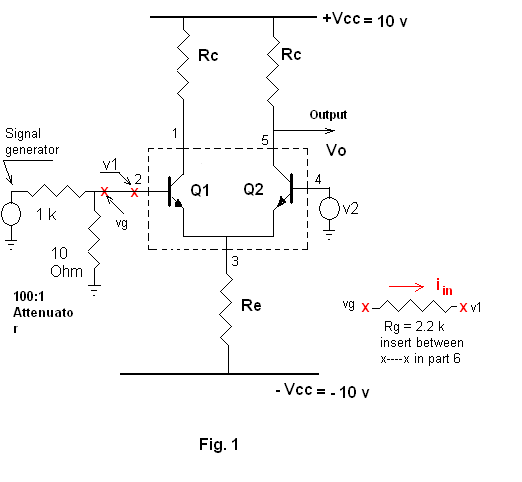
V1 (pp) = 25 mVpp, vo (pp) = 1.105 Vpp , AD = 1.105 Vpp / 25 mVpp = 44.2

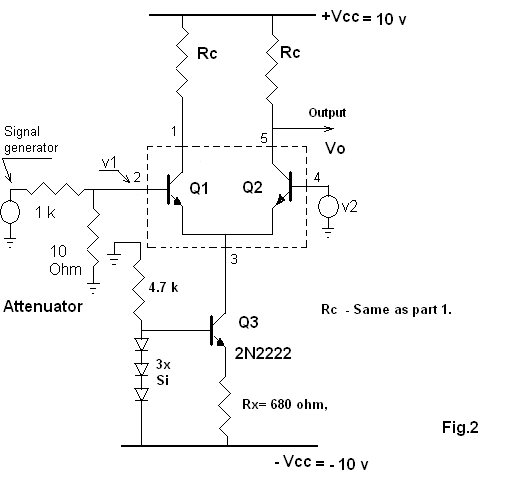
Common mode result: v1,2(com) = 23.824 mVpp, vo­(com) = -1.102V < 1mVpp may be 0.2 mVpp

(See photo)

AD = 1.102 Vpp/23.824 mVpp = 46.3, ACOM = 0.2 mVpp / 23.824 mVpp = 0.0084 (with current source)

CMRR = 20 log AD / ACOM = 20 log (46.3 / 0.0084) = 74.8 dB





**Conclusion:**

As a result of this lab, I was able to better understand constructing DC coupled differential amplifiers by using NPN-BJTs. I was able to measure the differential and common-mode voltage gains, the common-mode rejection ratio, as well as simulate AC small signal analysis on the circuit shown in Fig 1 and Fig 2. As mentioned in the lab procedure, a differential amplifier is a directly coupled active circuit with two independent input drives (V1 & V2) and a signal dependent output (Vo). V1 is called the non-inverting input and the other V2 as the inverting one. In general, the output is the product of the non-inverting and inverting gains of each input. Under a large signal condition, Vo is not a linear function of V1 and V2. It was interesting to note that when VCOM is lowered the common-mode voltage gains were lowered making the total voltage gain higher. In the later parts of the lab, we also defined the common-mode rejection ratio which is the ratio of AD and ACOM.